Figure 1

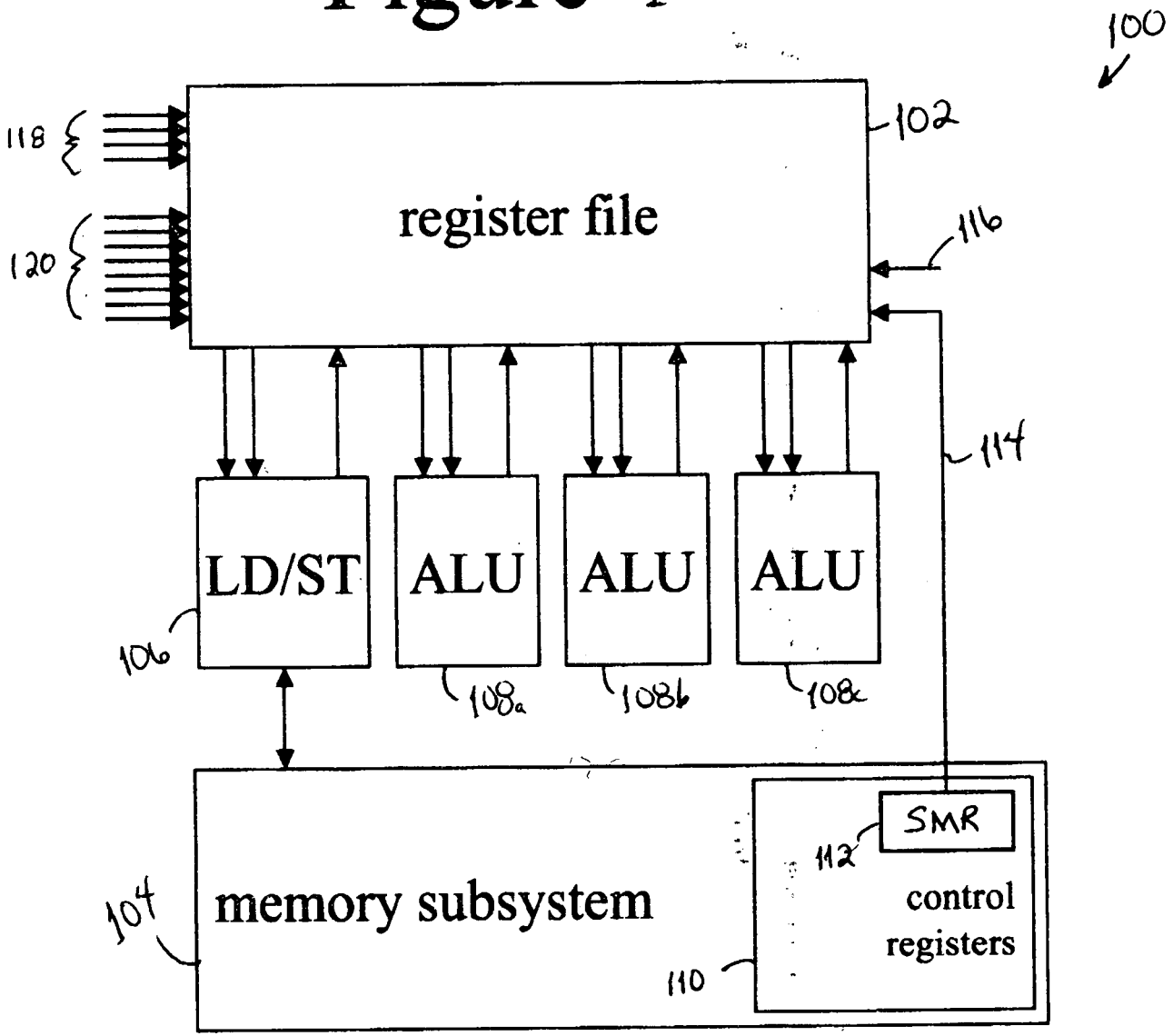

100
118
120
register file
102
116
114
LD/ST
ALU
ALU
ALU
106
108a
108b
108c
memory subsystem
104
SMR
112
control registers
110

Figure 2

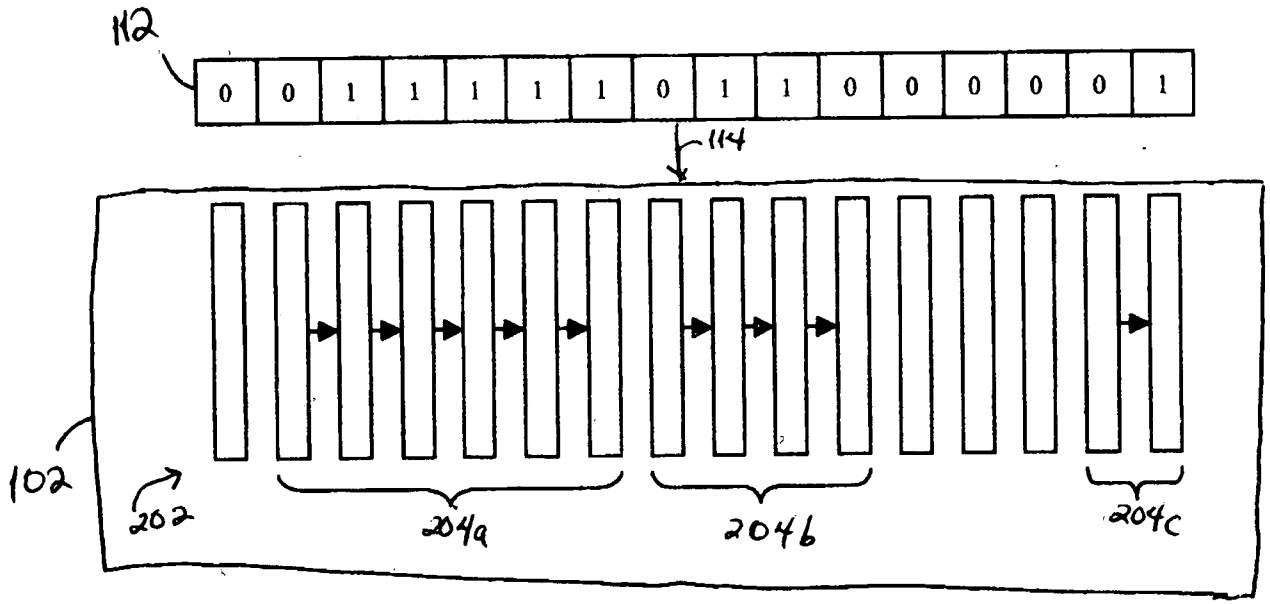


Figure 3

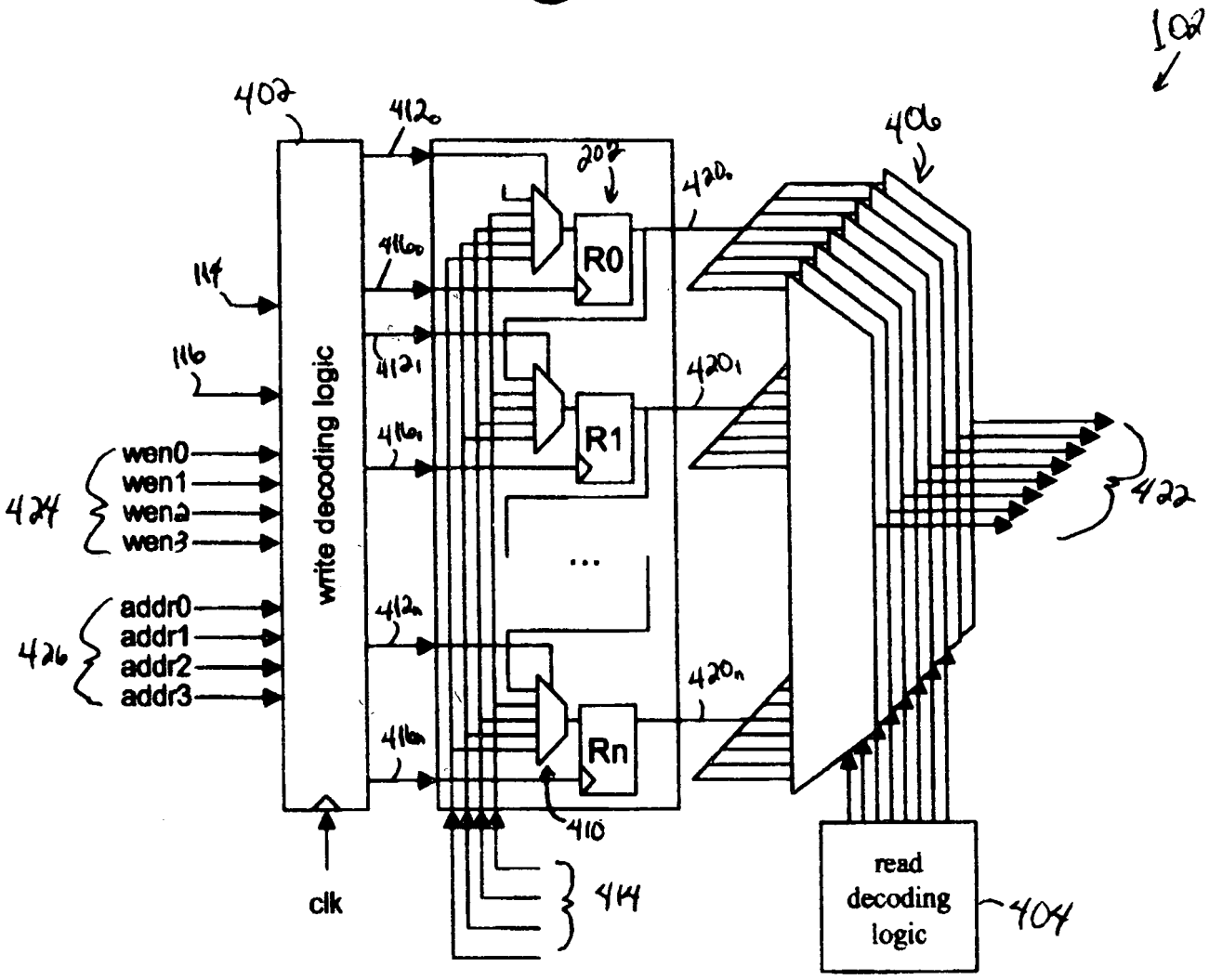
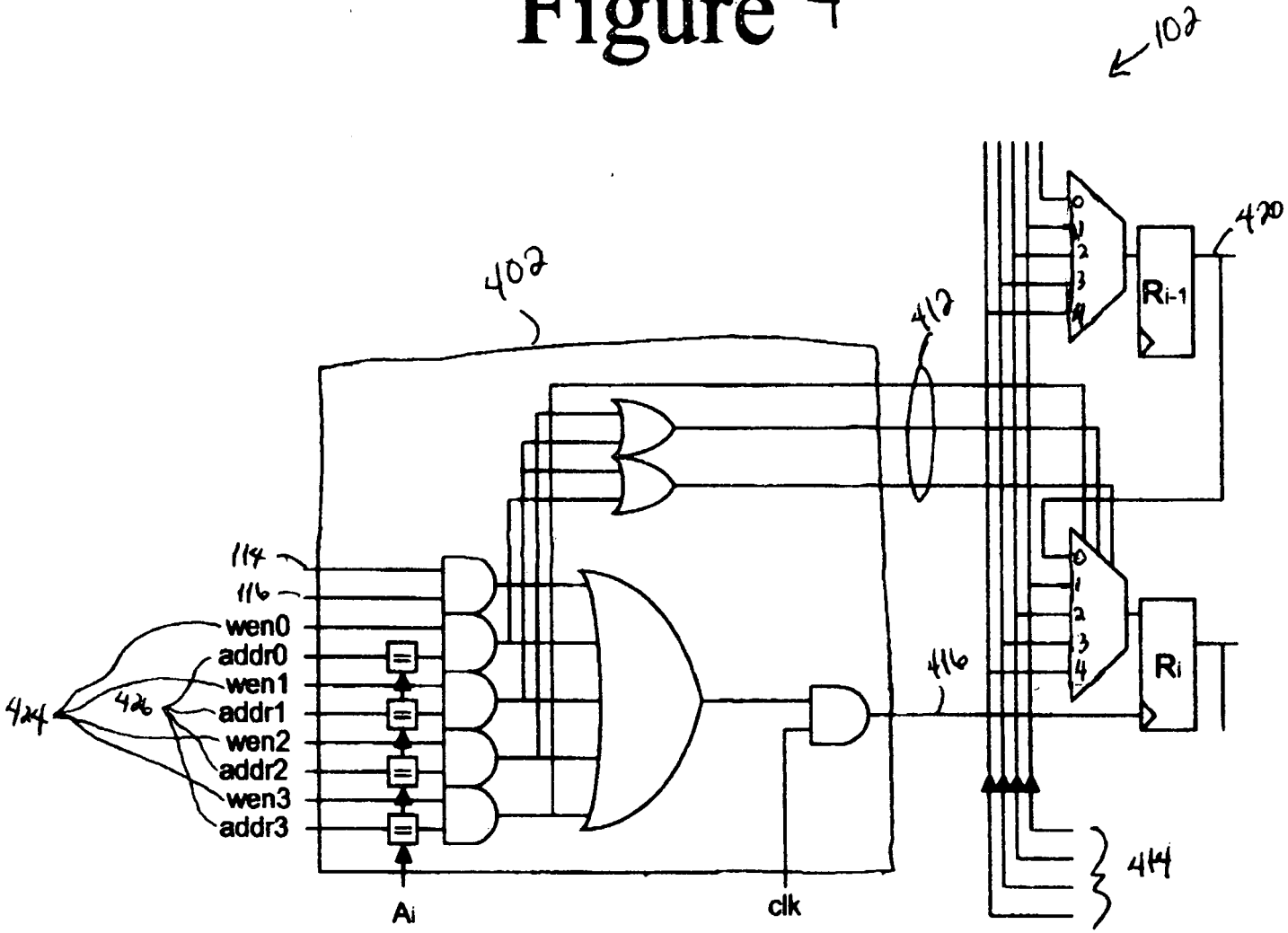

102
402
412₀
406
202
420₀
R0
416₀
114
116
write decoding logic
412₁
420₁
R1
416₁
wen0
wen1
wen2
wen3
424
...
422
addr0
addr1
addr2
addr3
426
412n
420n
Rn
416n
410
clk
414
read decoding logic
404

Figure 4


102
402
412
420
Ri-1
Ri
114
116
wen0
addr0
wen1
addr1
wen2
addr2
wen3
addr3
424
426
416
414
Ai
clk

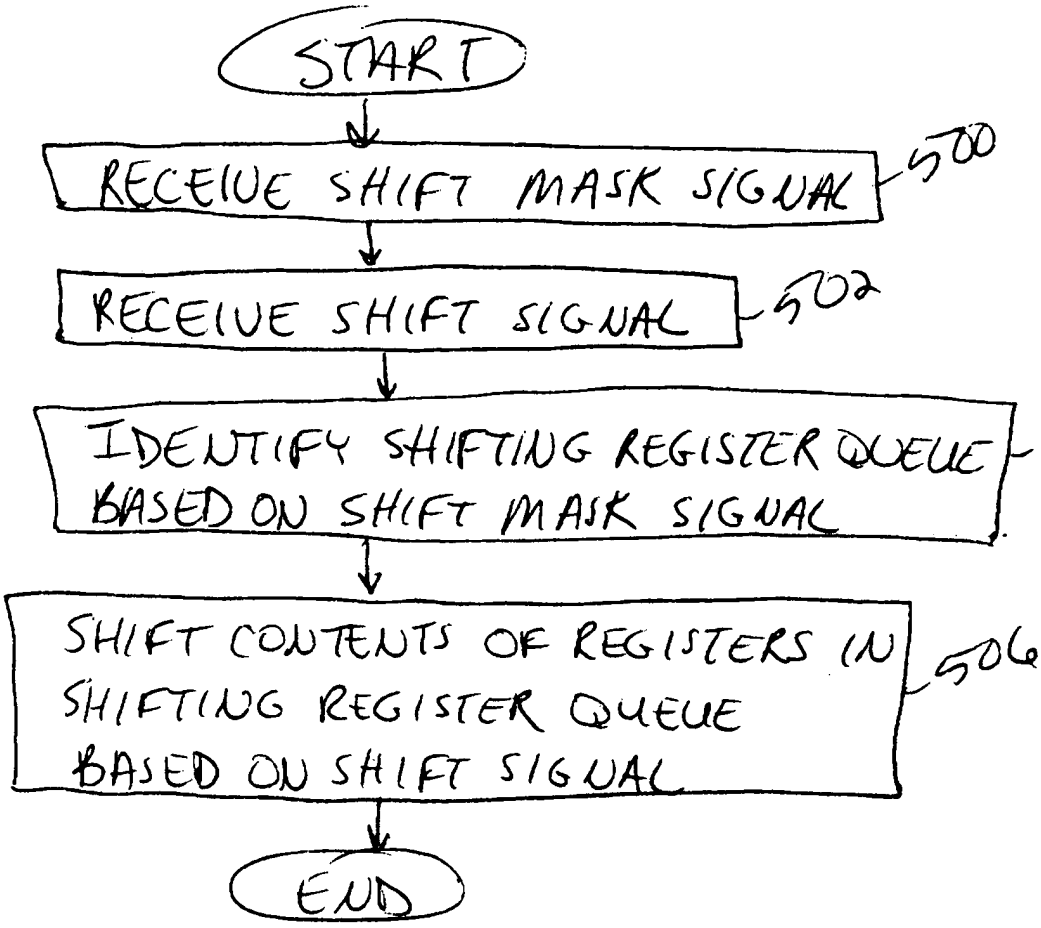

START
RECEIVE SHIFT MASK SIGNAL
500
RECEIVE SHIFT SIGNAL
502
IDENTIFY SHIFTING REGISTER QUEUE BASED ON SHIFT MASK SIGNAL
504
SHIFT CONTENTS OF REGISTERS IN SHIFTING REGISTER QUEUE BASED ON SHIFT SIGNAL
506
END

FIGURE 5